Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec– 2017**

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| **Code :** | **14EC2016** | **Duration :** | **3hrs** |
| **Sub. Name :** | **CAD FOR ELECTRONICS ENGINEERS** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Default value of net type os assigned as \_\_\_\_\_\_\_\_. | CO3 | 1 |
| b. | What statement and data type is used in dataflow and structural modeling Explain with examples? | CO3 | 2 |
| c. | Write a note initial and always block statement? | CO3 | 2 |
| d. | Implement a 1\*4 demux using behavioral modelling techniques? | CO3 | 5 |
| e. | Explain Floor planning and their techniques in detail. | CO3 | 10 |
| (OR) | | | | |
| 2. | a. | \_\_\_\_\_\_\_\_\_\_\_\_\_can be used for modelling both combinational and sequential. | CO3 | 1 |
| b. | What is the difference between wire and reg? | CO3 | 1 |
| c. | List all the net types and register data types in Verilog. | CO3 | 2 |
| d. | Explain with suitable examples on data types and data operators in Verilog, | CO3 | 8 |
| e. | With suitable example User defined primitives and User defined functions. | CO3 | 8 |
|  |  |  |  |  |
| 3. | a. | Sketch FOR loop. | CO1 | 1 |
|  | b. | Under what circumstances are for loop used? | CO1 | 1 |
|  | c. | Differentiate between pretest mode and post test mode. | CO1 | 2 |
|  | d. | What is structure tunnel? | CO1 | 2 |
|  | e. | Create a 1-D numeric array which consists of ten elements and rotate it ten times. For each rotation display the equivalent binary numbers of the first array element in the form of Boolean array. Also List down the steps to be followed. | CO1 | 14 |
| (OR) | | | | |
| 4. | a. | What is looping in LabVIEW? State the advantage of looping. | CO2 | 1 |
|  | b. | What is tunnel? How it's used in loops? | CO2 | 1 |
|  | c. | What are the different types of loops used in LabVIEW? | CO2 | 2 |
|  | d. | What is while loop? Under what circumstances are while loop used? | CO2 | 2 |
|  | e. | What is while loop? Under what circumstances are while loop used? | CO2 | 14 |
|  |  |  |  |  |
| 5. | a. | Explain about constructors in MATLAB with an example. Also explain the steps in checking its output in command window. | CO1 | 15 |
|  | b. | Write a MATLAB class program to read from a file. | CO1 | 5 |
| (OR) | | | | |
| 6. | a. | Explain the concept of Binary search algorithm with a MATLAB class program. | CO1 | 15 |
|  | b. | Explain about the features of Object Oriented Programming in MATLAB. | CO1 | 5 |
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| 7. | a. | What is modular programming? | CO2 | 1 |
|  | b. | Define Sub –VI in LabVIEW. | CO2 | 1 |
|  | c. | Explain the need of icon and connector pane. | CO2 | 2 |
|  | d. | What is default icon and custom icon? | CO2 | 2 |
|  | e. | Create a VI to find the radians for the given degrees and convert a section of VI in to a sub VI. List down the steps to be followed. | CO2 | 14 |
| (OR) | | | | |
| 8. | a. | Acronym of LabVIEW \_\_\_\_\_\_\_\_\_\_\_\_\_. | CO2 | 1 |
|  | b. | Write down the type of cluster in LabVIEW. | CO2 | 1 |
|  | c. | List down the steps to create a 1 D numeric array. | CO2 | 2 |
|  | d. | Create a VI block diagram to change color of R, G, and B elements in a pixel. | CO2 | 2 |
|  | e. | Create a sub VI to compute the average of five student marks. Build a VI o generate 100 random numbers between 0 to 1 using for Loop. Also List down the steps to be followed. | CO2 | 14 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Which level of abstraction level is available in Verilog but not in VHDL? | CO3 | 1 |
|  | b. | Which logic level is not supported by Verilog? | CO3 | 1 |
|  | c. | Name the Routing algorithms. | CO3 | 2 |
|  | d. | With suitable example User defined primitives and User defined functions. | CO3 | 8 |
|  | e. | Explain with suitable examples Control, Loop and decision statements in Verilog | CO3 | 8 |

ALL THE BEST